PAD LABELS 1/3 — DIGITAL & CONTROL (north edge, 27 pads)

VDD domain (1.2 V). Coordinates: y = +1435 µm, x from −330 (CLK) to +1750 (GND) in 80 µm steps — left to right in the table order

Label	Pads	Dir	Function
CLK	1	in	System clock for the digital core (sequencer, SPI-independent). One decision slot = 12 clock cycles (SLOT_DIV); operating frequency not yet fixed in the spec (50 vs 100 MHz open item).
RST_N	1	in	Active-low asynchronous reset of the digital core (sequencer state, weight latches, spin register).
SCLK · CSN · MOSI	3	in	SPI slave, mode 0, CRC-16: loads the 544 weights, the SCHED table, NSPIN and control registers (RUN / QUENCH).
MISO	1	out	SPI read-back: the 16-bit spin register (the answer), status / DONE, register contents.
DBG_STB	1	out	Debug: the comparator sample strobe itself, one pulse per slot. An external instrument samples DBG_CMP on this edge.
DBG_CMP	1	out	Debug: the raw comparator decision latched at each strobe — the spin-decision stream before it is written to the register (for randomness / autocorrelation measurement).
CP_EN	1	out	eFlash program controller (ppu_pgm_ctrl): charge-pump enable. No flash cell on this chip — the pin is exposed for the future eFlash bring-up.
PGM_PULSE	1	out	eFlash ISPP program pulse (incremental-step pulse programming) from ppu_pgm_ctrl. Unused internally on Version A.
PLANE_SEL	1	out	eFlash plane select: 0 = J+ plane, 1 = J− plane, during program / erase-verify. Unused internally on Version A.
CP_READY	1	in	Charge-pump ready handshake into ppu_pgm_ctrl. ⚠ No internal pull-up: must be driven on the board (tie low if unused).
VFY_LEVEL[5:0]	6	in	6-bit verify (read-back Vt level) into the ISPP loop. ⚠ No internal pull-up: must be driven on the board (tie low if unused).
SCAN_EN · SI · SO · CK	4	rsv	Reserved / not connected: the digital core has no scan chain (open item). Pads kept for pin-compatibility with a later revision.
DONE_IRQ	1	rsv	Reserved / not connected: DONE is read through the SPI status register on Version A.
VDD	2	pwr	1.2 V digital supply (two of the four VDD pads; the other two are on the east edge). RC-triggered power clamp XCL_VDD.
GND	2	gnd	Ground (two of the eight real GND pads).

Sources: DELIVERY.md §2 pinout (generated from gen_pad_ring.py), ppu_digital_top.v, ppu_pgm_ctrl.v, ppu_atest.scs, ANALOG_SPEC.md, ESD_REPORT.md · labels verified in ppu65_chip.gds (layers 139/136/137) · 10 Sep 2026

PAD LABELS 2/3 — ANALOG TRIM & REFERENCE (west edge 18 pads + 6 on the south)

AVDD_REF domain (2.5 V). West: x = −525 µm, y from −115 (AVDD_REF) to +1245 (VCM_B2); south trims at y = −305 µm, x = 150 … 550

Label	Pads	Dir	Function
AVDD_REF	2 (W)	pwr	2.5 V supply of the reference block: bandgap (0.927 V) → master bias (10 µA seed) → R-string taps → buffers. Bridged to AVDD by anti-parallel ESD diodes; clamp XCL_REF.
GND	1 (W)	gnd	Ground pad of the west edge.
BSEL[2:0]	3 (W)	in	Selects one of 8 BREFT taps = the comparator reference BREF (0.5927 → 0.6345 V, ≈ 6 mV/step). A PER-PROBLEM setting: the compiler picks the tap that centres the decision threshold (e.g. code 7 for the N = 35 deck).
VBIAS_B[2:0]	3 (W)	trim	8-tap trim of VBIAS = gate of every synapse current source (0.5394 V nominal). Sets the size of one weight unit (≈ 6.7–7.4 µA): the α knob of the whole array.
VREFSL_B[2:0]	3 (W)	trim	8-tap trim of VREF_SL = the level the conveyors hold both source lines at (0.150 V). Keeps the array summation linear (without it: 35 % compression).
VREADR_B[2:0]	3 (W)	trim	8-tap trim of V_READ = the bit-line voltage a selected row is driven to (0.499 V).
VCM_B[2:0]	3 (W)	trim	8-tap trim of VCM = input common mode of the thermal-noise chain (A1 gates, 0.8975 V; target 0.900 V, full window scanned post-layout).
VCASC_B[2:0]	3 (S)	trim	8-tap trim of VCASC = cascode bias of the fold's current mirror (≈ 0.75 V; PEX taps 755.8–773.3 mV, 2.49 mV/step). Sets the mirror's output impedance / copy accuracy.
BANC_B[2:0]	3 (S)	trim	8-tap trim of BANC = the fold's fixed anchor (0.620 V; PEX taps 623.0–641.0 mV, 2.58 mV/step, 18.0 mV range). The PER-CHIP comparator-offset trim knob (nominal code 3).

All 18 trim bits are real chip ports (18 of the 54 ports in syn_chip.cdl): if the board does not drive them the gates float and the trim code is undefined — the chip cannot be measured. Trims are set once per chip; BSEL is set once per problem.

Sources: DELIVERY.md §2 pinout (generated from gen_pad_ring.py), ppu_digital_top.v, ppu_pgm_ctrl.v, ppu_atest.scs, ANALOG_SPEC.md, ESD_REPORT.md · labels verified in ppu65_chip.gds (layers 139/136/137) · 10 Sep 2026

PAD LABELS 3/3 — SUPPLIES, GROUNDS & ANALOG TEST (east edge 8 pads + south 8)

Four supply domains: VDD 1.2 V (digital) · AVDD 2.5 V (array & analog) · AVDD_REF 2.5 V (references) · VWL_F 1.0 V (word lines)

Label	Pads	Dir	Function
AVDD	3 (E1, S2)	pwr	2.5 V analog supply: synapse array, conveyors, fold, StrongARM comparator, noise chain, level shifters. Clamp XCL_AVDD (nch_25, 3000 µm).
VDD	4 (N2, E2)	pwr	1.2 V digital supply (SPI, regfile, sequencer, weight latches, spin register). Clamp XCL_VDD (nch_hvt, 2400 µm).
VWL_F	1 (E)	pwr	1.0 V word-line supply, FORCE side: powers the WL drivers; WL high = 1.0 V is the spin '1' level seen by the synapse switches. Clamp XCL_VWL.
VWL_S	1 (E)	ana	Kelvin SENSE of the same word-line supply: carries no current; joins VWL_F at the board's star point so the regulator sees the on-chip voltage.
GND	8 (N2, E3, S2, W1)	gnd	Single ground net for digital and analog (separation is done on the board). Substrate is tied via the seal-ring P+ tap.
ATOUT	1 (S)	ana	Analog test-mux OUTPUT: 16 internal nodes (SLP, SLN, BSENSE, bias rails …) selected one-hot by the SPI register atest_en[15:0] → 16 nsw switches → buffer → pad.
ATB	1 (S)	ana	Analog Test Bus: the raw node where the 16 test switches meet, before the buffer — direct (unbuffered) access to the selected node.
ATOUT2	1 (S)	rsv	Reserved / not connected (second test output, unused on Version A).
VSUB	1 (S)	nc	⚠ NOT CONNECTED inside the chip (LVS: the only pass-through net, zero devices) and no ESD diode. The substrate is grounded through the seal ring, not this pad. The board must NOT count it as a ground pad.

Totals: 67 pads = 27 N + 8 E + 14 S + 18 W · 4 supply domains + 8 GND · 48 signal pads with dual ESD diodes · every pad carries its label on the M9/M6/M7 pin layer (verified: 67/67).

Sources: DELIVERY.md §2 pinout (generated from gen_pad_ring.py), ppu_digital_top.v, ppu_pgm_ctrl.v, ppu_atest.scs, ANALOG_SPEC.md, ESD_REPORT.md · labels verified in ppu65_chip.gds (layers 139/136/137) · 10 Sep 2026